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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	10595384
Filing Date	2006-04-13
First Named Inventor	Christopher Hess
Art Unit	2857
Examiner Name	
Attorney Docket Number	D5116-00051

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	1	Stapper, C. H., Rosner, R. J., "Integrated Circuit Yield Management and Yield Analysis: Development and Implementation," IEEE Transactions on Semiconductor Manufacturing, pp. 95-102, Vol. 8, No. 2, 1995	☐
	2	Ipri, A. C., Sarace, J. C., "Integrated Circuit Process and Design Rule Evaluation Techniques," RCA Review, pp. 323-350, Volume 38, Number 3, September 1977	☐
	3	Buehler, M. G., "Microelectronic Test Chips for VLSI Electronics," VLSI Electronics Microstructure Science, pp. 529-576, Vol. 6, Chapter 9, Academic Press, 1983	☐
	4	Doong, K., Cheng, J., Hsu, C., "Design and Simulation of Addressable Failure Site Test Structure for IC Process Control Monitor," pp. 219-222, International Symposium on Semiconductor Manufacturing, 1999	☐
	5	Hess, C., Weiland, L. H., "Influence of Short Circuits on Data of Contact & Via Open Circuits Determined by a Novel Weave Test Structure," IEEE Transactions on Semiconductor Manufacturing, pp. 27-34, Vol. 9, No. 1, 1996	☐
	6	Hess, C., Stashower, D., Stine, B. E., Weiland, L. H., Verma, G., Miyamoto, K., Inoue, K., "Fast Extraction of Defect Size Distribution Using a Single Layer Short Flow NEST Structure", IEEE Transactions on Semiconductor Manufacturing, pp. 330-337, Vol. 14, No. 4, 2001	☐
	7	Walton, A. J., Ward, D., Robertson, J. M., Holwill R. J., "A Novel Approach for an Electrical Vernier to Measure Mask Misalignment", pp. 950-953, 19th European Solid State Device Research Conference ESSDERC '89, Springer Verlag, 1989	☐
	8	Hess, C., Stine, B. E., Weiland, L. H., Mitchell, T., Karnett, M., Gardner, K., "Passive Multiplexer Test Structure For Fast and Accurate Contact and Via Fail Rate Evaluation", pp. 163-167, Proc. International Conference on Microelectronic Test Structures (ICMTS), Vol. 15, Cork (Ireland), 2002	☐
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	10	Hess, C., Weiland, L. H., Bornefeld, R., "Customized Checkerboard Test Structures to Localize Interconnection Point Defects", Proc. VLSI Multilevel Interconnection Conference (VMIC), pp. 163-168, Santa Clara (USA), 1997	☐

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	11	Hess, C., Weiland, L. H., "Defect Parameter Extraction in Backend Process Steps using a Multilayer Checkerboard Test Structure", Proc. International Conference on Microelectronic Test Structures (ICMTS), pp. 51-56, Nara (Japan), 1995	☐
	12	Hess, C., Weiland, L. H., "Strategy to Disentangle Multiple Faults to Identify Random Defects within Test Structures", Proc. International Conference on Microelectronic Test Structures (ICMTS), pp. 141-146, Kanazawa (Japan), 1998	☐
	13	Hess, C., Weiland, L. H., "Harp Test Structure to Electrically Determine Size Distributions of Killer Defects", IEEE Transactions on Semiconductor Manufacturing, pp. 194-203, Vol. 11, No. 2, 1998	☐
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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Richard A. Paikoff/	Date (YYYY-MM-DD)	2007-08-15
Name/Print	Richard A. Paikoff	Registration Number	34,892

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